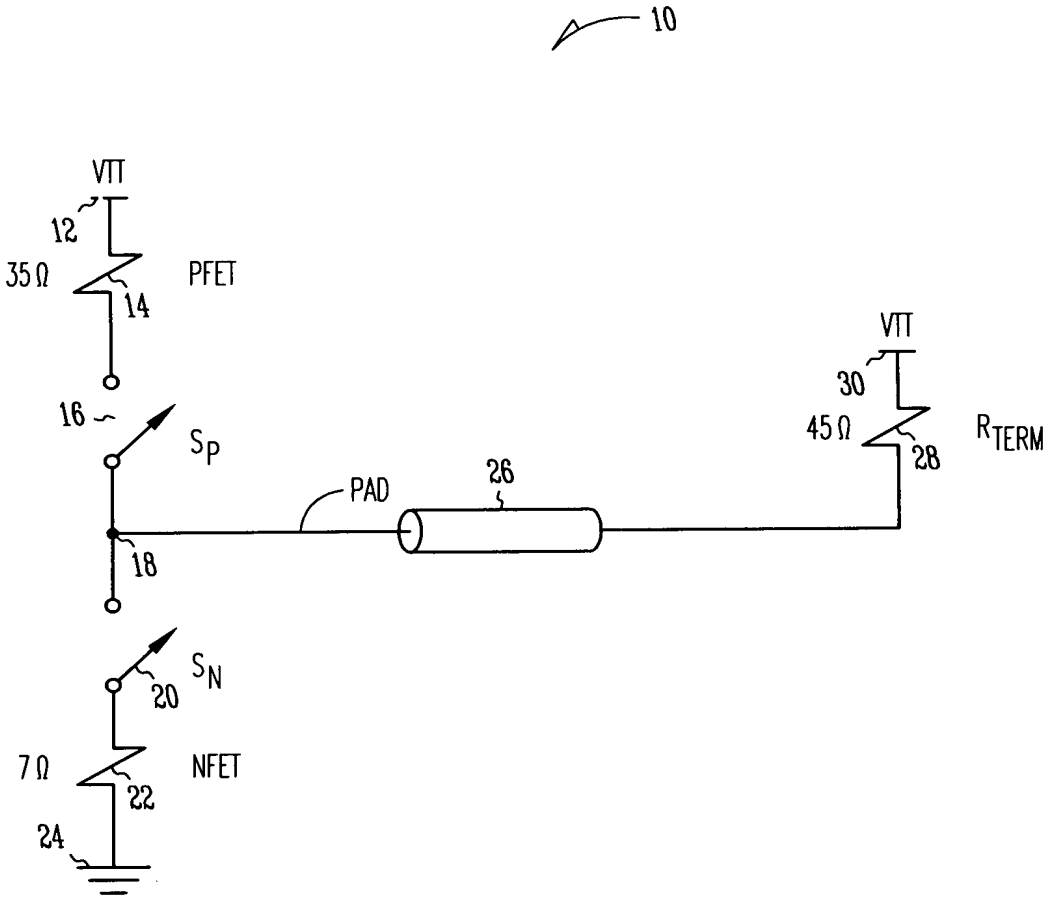

10
VTT
12
35 Ω
PFET
14
16
$S_P$
18
PAD
26
VTT
30
45 Ω
28
$R_{TERM}$
$S_N$
20
7 Ω
NFET
22
24

Fig.1

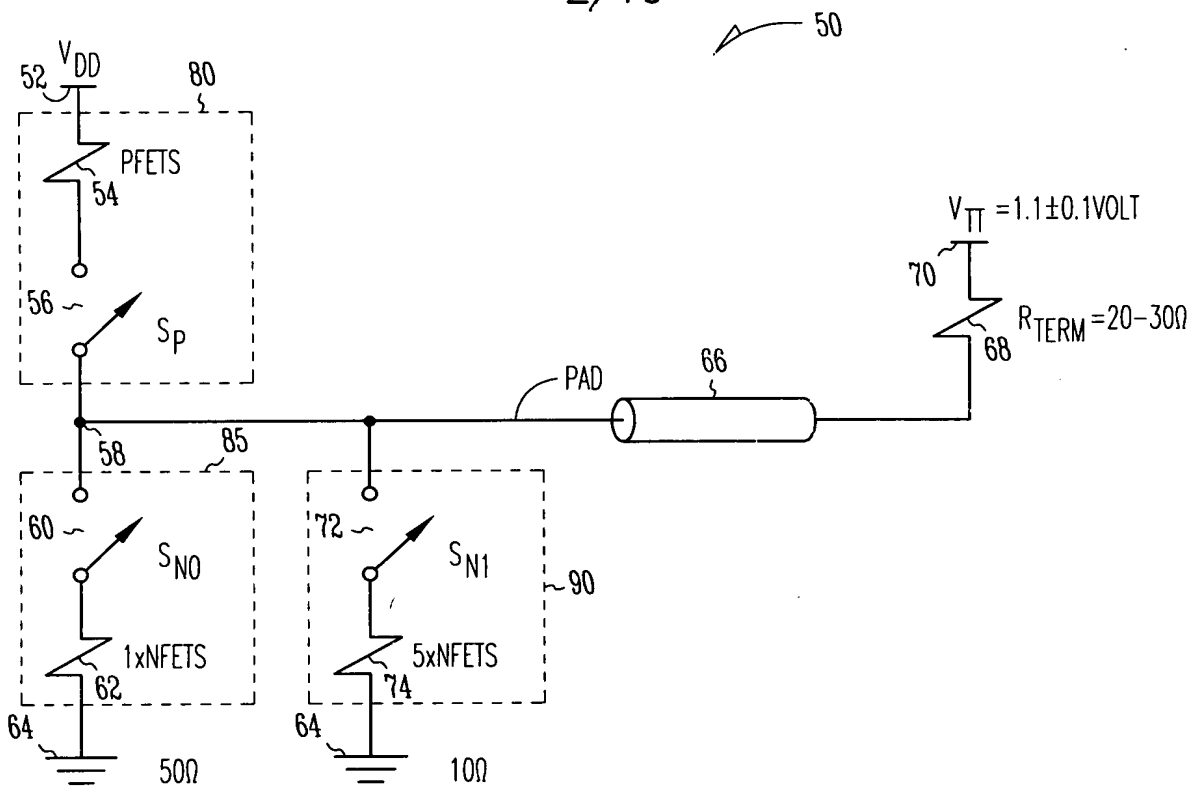

50
52
$V_{DD}$
80
PFETS
54
56
$S_P$
$V_{TT}$ =1.1±0.1VOLT
70
$R_{TERM}$=20-30Ω
68
PAD
66
58
85
60
$S_{NO}$
1xNFETS
62
64
50Ω
72
$S_{N1}$
90
5xNFETS
74
64
10Ω

Fig.2A

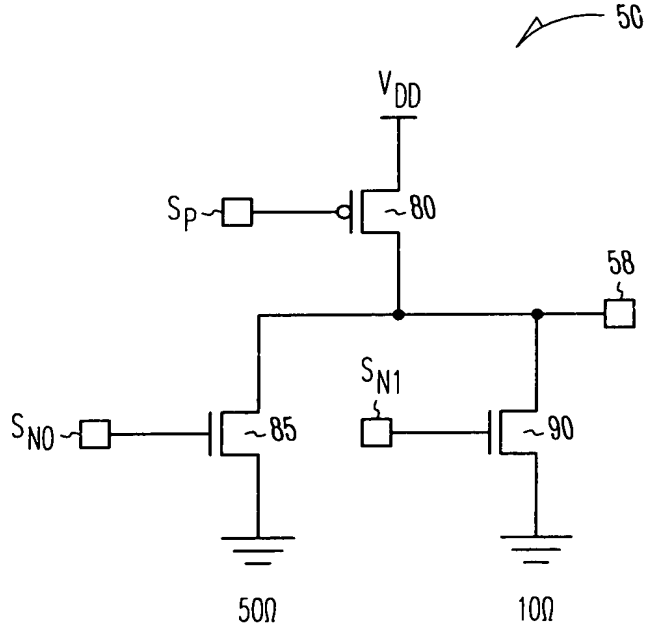

50
$V_{DD}$
$S_P$
80
58
$S_{N1}$
$S_{NO}$
85
90
50Ω
10Ω

Fig.2B

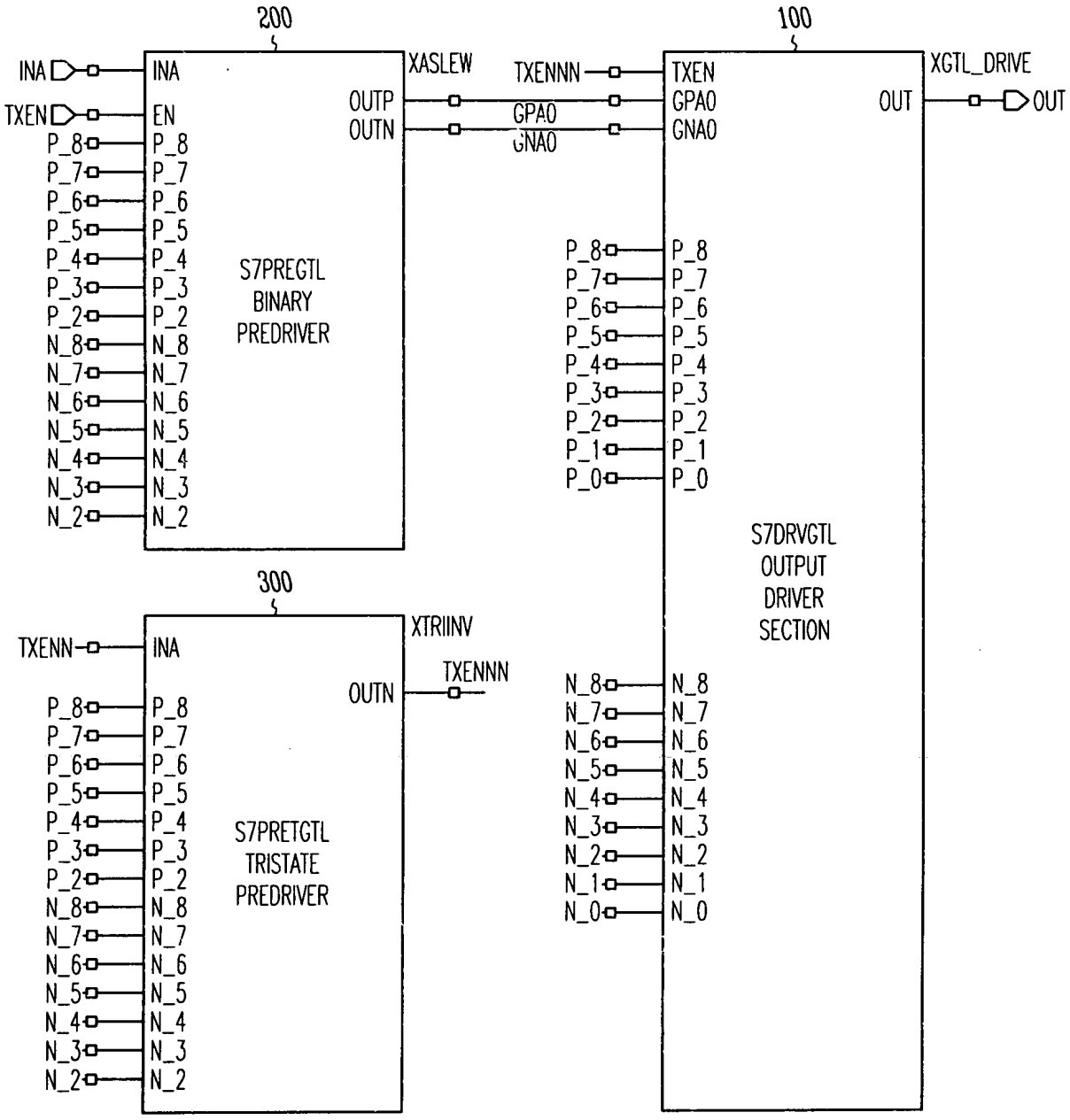

200
INA
TXEN
P_8
P_7
P_6
P_5
P_4
P_3
P_2
N_8
N_7
N_6
N_5
N_4
N_3
N_2
INA
EN
P_8
P_7
P_6
P_5
P_4
P_3
P_2
N_8
N_7
N_6
N_5
N_4
N_3
N_2
S7PREGTL
BINARY
PREDRIVER
XASLEW
OUTP
OUTN
100
TXENNN
GPA0
GNA0
TXEN
GPA0
GNA0
P_8
P_7
P_6
P_5
P_4
P_3
P_2
P_1
P_0
N_8
N_7
N_6
N_5
N_4
N_3
N_2
N_1
N_0
S7DRVGTL
OUTPUT
DRIVER
SECTION
XGTL_DRIVE
OUT
OUT
300
TXENN
INA
P_8
P_7
P_6
P_5
P_4
P_3
P_2
N_8
N_7
N_6
N_5
N_4
N_3
N_2
S7PRETGTL
TRISTATE
PREDRIVER
XTRIINV
OUTN
TXENNN

Fig.3

TITLE: GTL + DRIVER
INVENTORS NAME: Rodney Ruesch
SERIAL NO.: 09/620,679



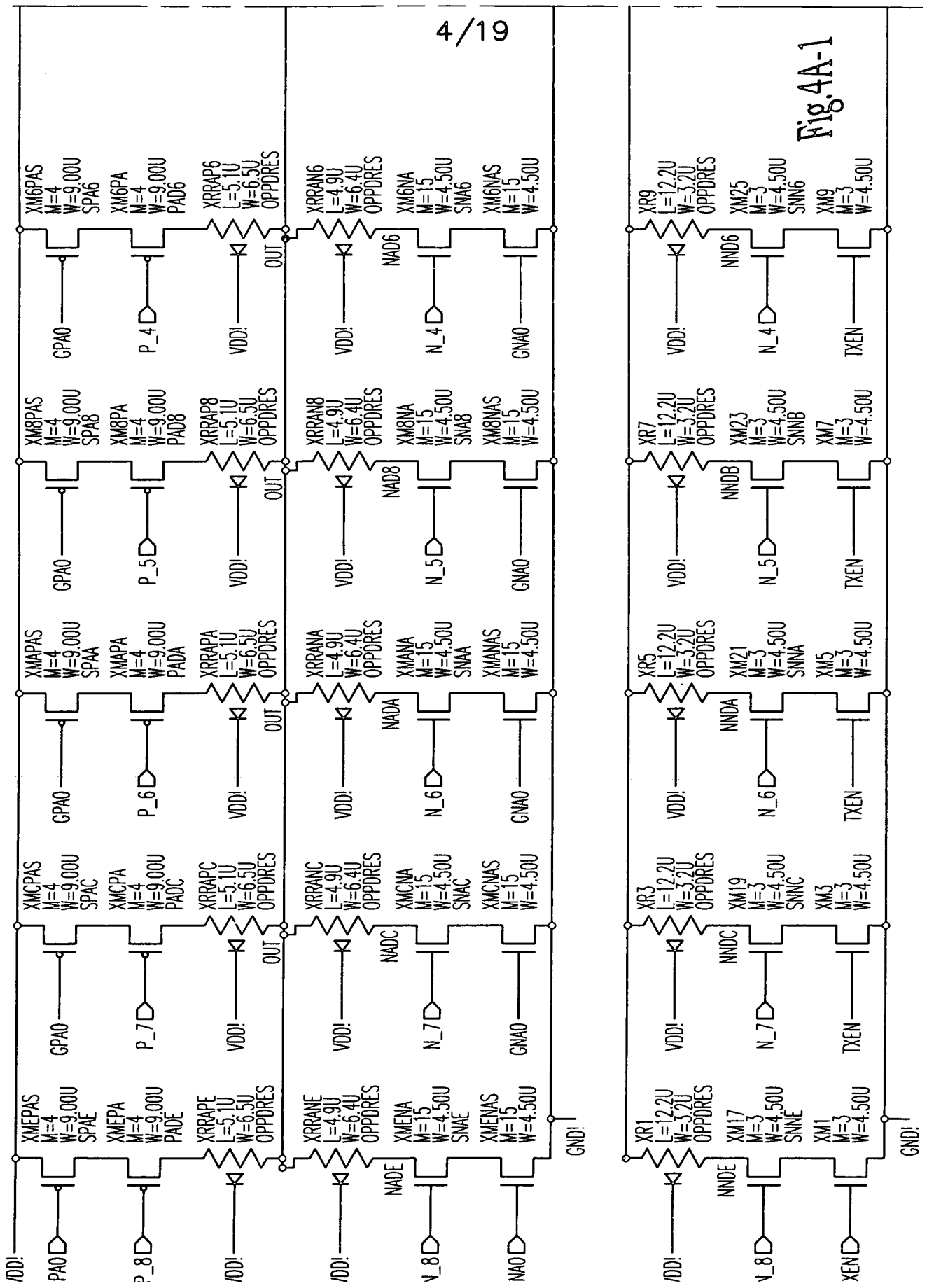



Fig.4A-1

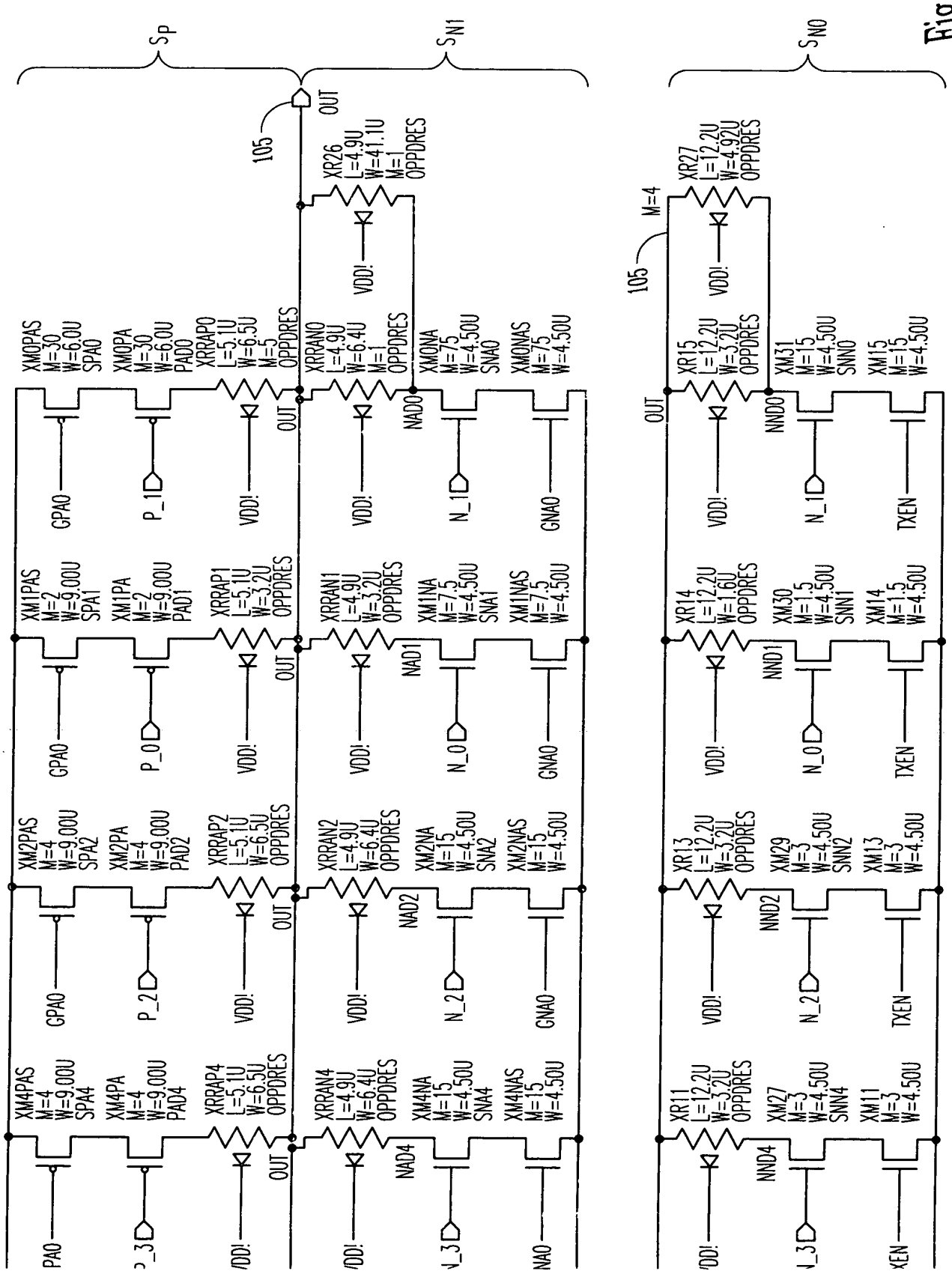

SP
SN1
SN0
105
OUT
XR26 L=4.9U W=41.1U M=1 OPPDRES
XR27 L=12.2U W=4.92U OPPDRES
M=4
XMOPAS M=30 W=6.0U SPA0
XMOPA M=30 W=6.0U PAD0
XRRAP0 L=5.1U W=6.5U M=5 OPPDRES
XRRAN0 L=4.9U W=6.4U M=1 OPPDRES
XMONA M=75 W=4.50U SNA0
XMONAS M=75 W=4.50U
XM1PAS M=2 W=9.00U SPA1
XM1PA M=2 W=9.00U PAD1
XRRAP1 L=5.1U W=3.2U OPPDRES
XRRAN1 L=4.9U W=3.2U OPPDRES
XM1NA M=7.5 W=4.50U SNA1
XM1NAS M=7.5 W=4.50U
XM2PAS M=4 W=9.00U SPA2
XM2PA M=4 W=9.00U PAD2
XRRAP2 L=5.1U W=6.5U OPPDRES
XRRAN2 L=4.9U W=6.4U OPPDRES
XM2NA M=15 W=4.50U SNA2
XM2NAS M=15 W=4.50U
XM4PAS M=4 W=9.00U SPA4
XM4PA M=4 W=9.00U PAD4
XRRAP4 L=5.1U W=6.5U OPPDRES
XRRAN4 L=4.9U W=6.4U OPPDRES
XM4NA M=15 W=4.50U SNA4
XM4NAS M=15 W=4.50U
XR15 L=12.2U W=3.2U OPPDRES
XM31 M=15 W=4.50U SNN0
XM15 M=15 W=4.50U
XR14 L=12.2U W=1.6U OPPDRES
XM30 M=1.5 W=4.50U SNN1
XM14 M=1.5 W=4.50U
XR13 L=12.2U W=3.2U OPPDRES
XM29 M=3 W=4.50U SNN2
XM13 M=3 W=4.50U
XR11 L=12.2U W=3.2U OPPDRES
XM27 M=3 W=4.50U SNN4
XM11 M=3 W=4.50U
VDD!
GPA0
P_1
P_0
P_2
P_3
N_1
N_0
N_2
N_3
GNA0
TXEN
NAD0
NAD1
NAD2
NAD4
NND0
NND1
NND2
NND4
PA0
NA0

Fig.4A-2

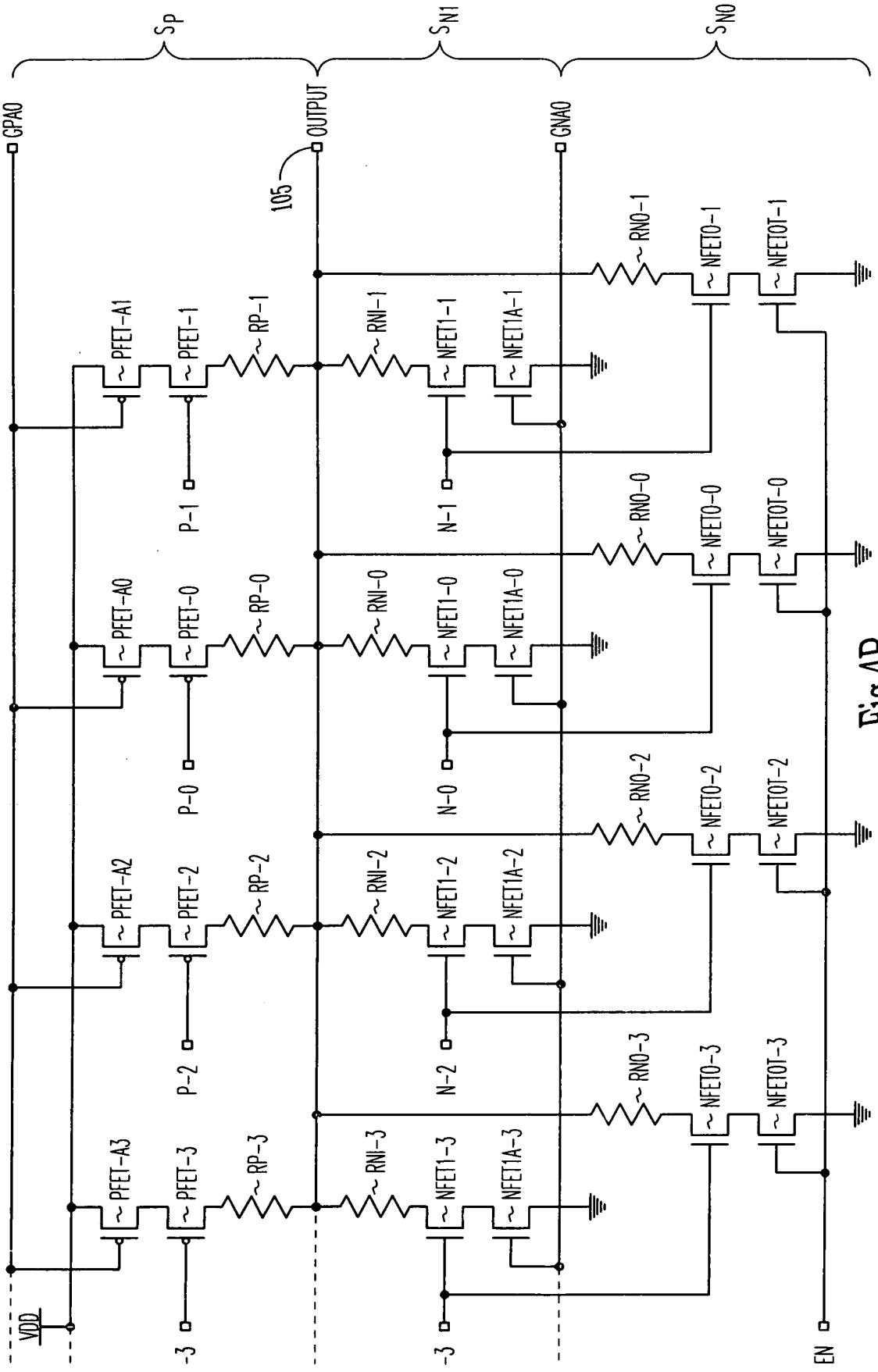
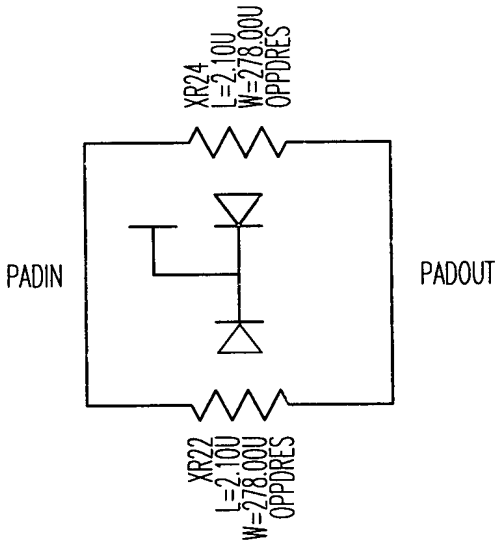

SP
SN1
SNO
GPAO
OUTPUT
GNAO
105
PFET-A1
PFET-1
RP-1
RNI-1
NFET1-1
NFET1A-1
RNO-1
NFETO-1
NFETOT-1
P-1
N-1
PFET-A0
PFET-0
RP-0
RNI-0
NFET1-0
NFET1A-0
RNO-0
NFETO-0
NFETOT-0
P-0
N-0
PFET-A2
PFET-2
RP-2
RNI-2
NFET1-2
NFET1A-2
RNO-2
NFETO-2
NFETOT-2
P-2
N-2
PFET-A3
PFET-3
RP-3
RNI-3
NFET1-3
NFET1A-3
RNO-3
NFETO-3
NFETOT-3
VDD
-3
-3
EN

Fig.4B



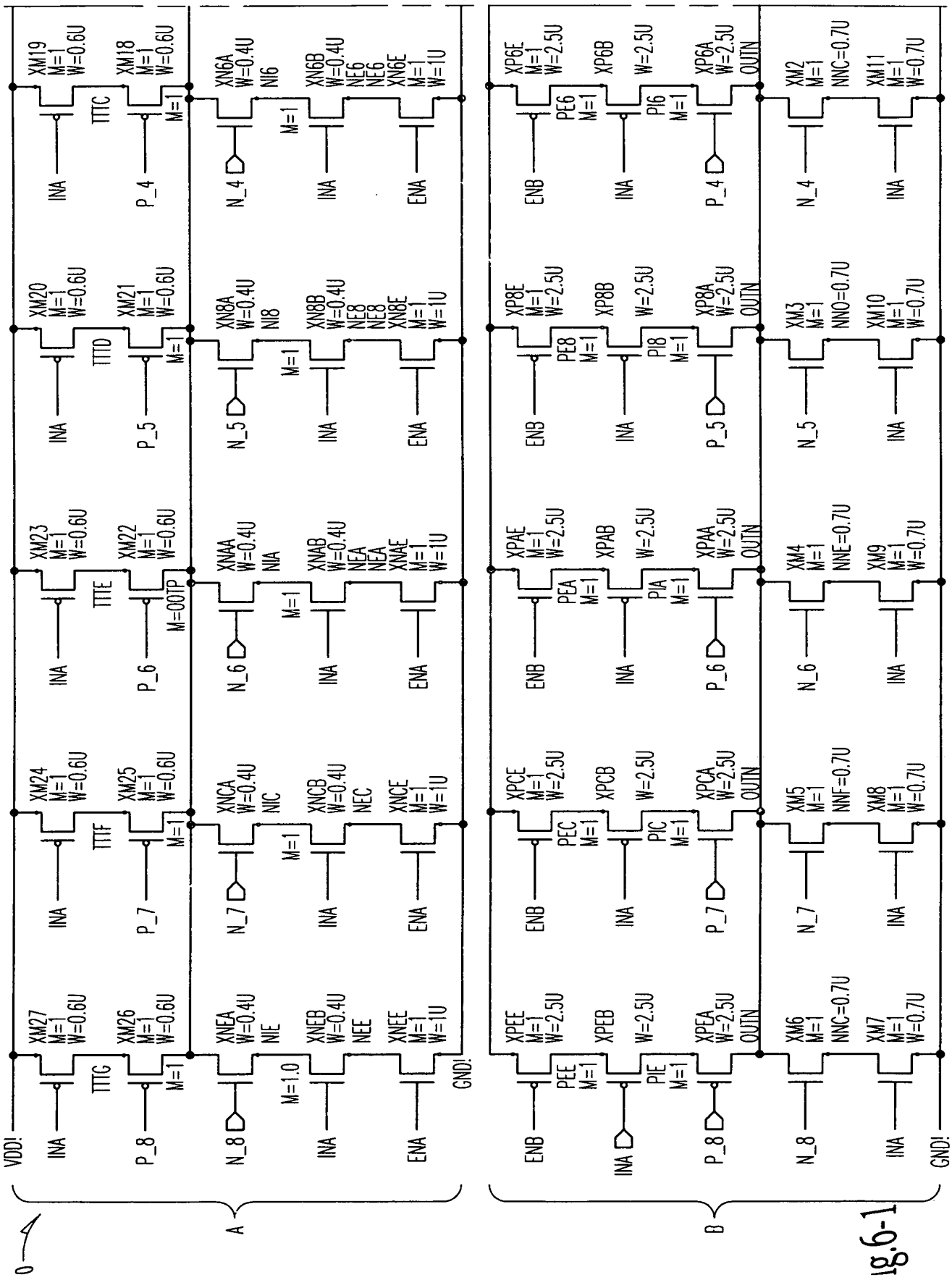

SELECTABLE OP RESISTORS TO BE USED WITH PADXFER METAL (LM) TOTAL RESISTANT MATCHING UP TO 3 OHMS

ONE RESISTOR L=2.1U AND W=93.0U = 3.0 OHMS
ONE RESISTOR L=2.1U AND W=111.0U = 2.5 OHMS
ONE RESISTOR L=2.1U AND W=139.0U = 2.0 OHMS
ONE RESISTOR L=2.1U AND W=185.0U = 1.5 OHMS
ONE RESISTOR L=2.1U AND W=278.0U = 1.0 OHMS
TWO RESISTORS L=2.1U AND W=278.0U IN PARALLEL = 0.5 OHMS SHOWN
ZERO RESISTORS TO BE USED FOR 0 OHMS

Fig.5

TITLE: GTL + DRIVER
INVENTORS NAME: Rodney Ruesch
SERIAL NO.: 09/620,679





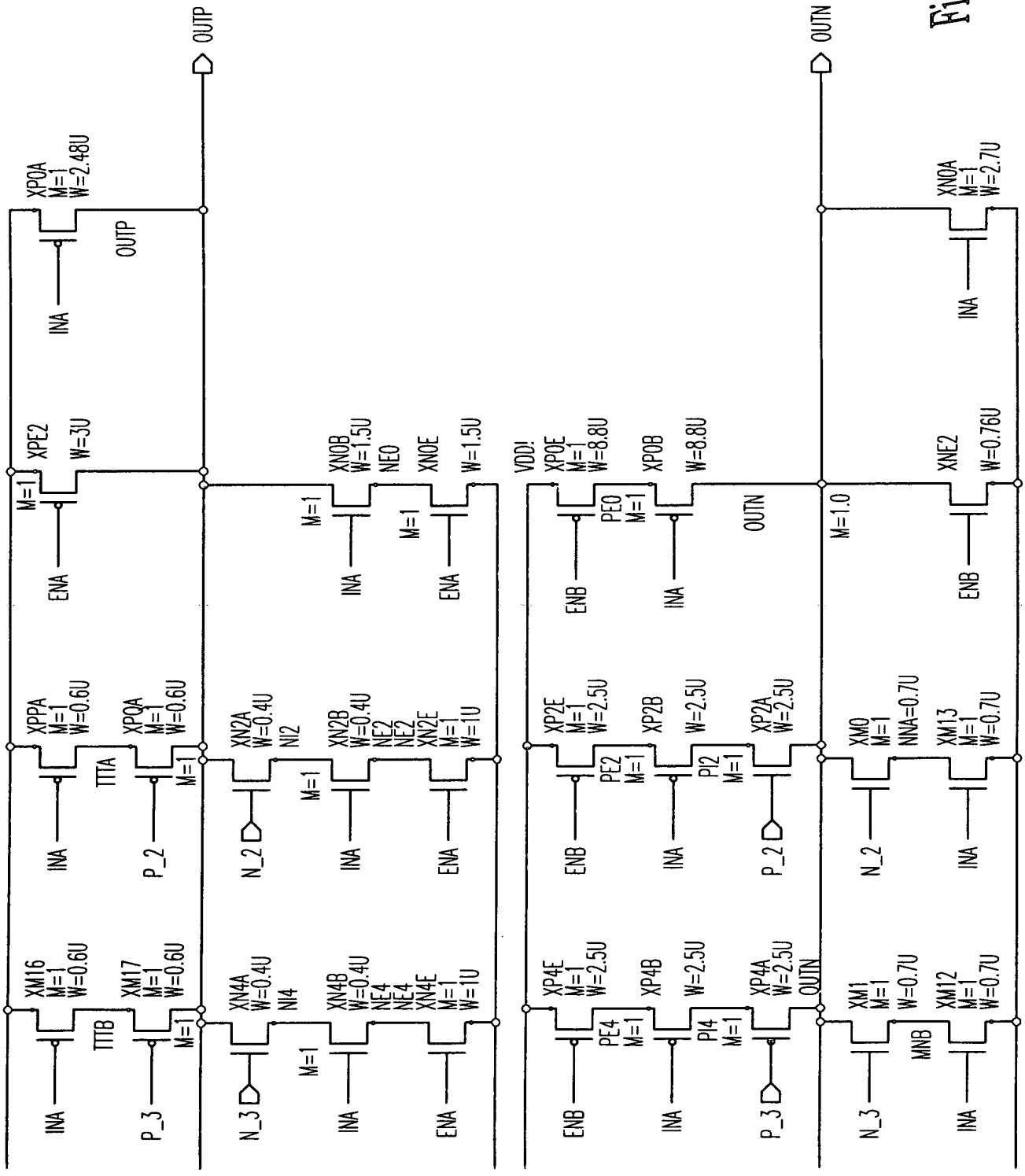

OUTP
XP0A M=1 W=2.48U
INA
OUTP
XPE2 W=3U
M=1
ENA
XPPA M=1 W=0.6U
INA
TTA
XPQA M=1 W=0.6U
P_2
M=1
XM16 M=1 W=0.6U
INA
TTB
XM17 M=1 W=0.6U
P_3
M=1
XN2A W=0.4U NI2
N_2
M=1
XN2B W=0.4U NE2 NE2
INA
XN2E M=1 W=1U
ENA
XN4A W=0.4U NI4
N_3
M=1
XN4B W=0.4U NE4 NE4
INA
XN4E M=1 W=1U
ENA
XN0B W=1.5U NE0
M=1
INA
XN0E W=1.5U
M=1
ENA
VDD!
XP0E M=1 W=8.8U
ENB
PE0 M=1
XP0B W=8.8U
INA
OUTN
XP2E M=1 W=2.5U
ENB
PE2 M=1
XP2B W=2.5U
INA
PI2 M=1
XP2A W=2.5U
P_2
XP4E M=1 W=2.5U
ENB
PE4 M=1
XP4B W=2.5U
INA
PI4 M=1
XP4A W=2.5U
P_3
OUTN
OUTN
XN0A M=1 W=2.7U
INA
M=1.0
XNE2 W=0.76U
ENB
XM0 M=1 NNA=0.7U
N_2
XM13 M=1 W=0.7U
INA
XM1 M=1 W=0.7U
N_3
MNB
XM12 M=1 W=0.7U
INA

Fig.6-2

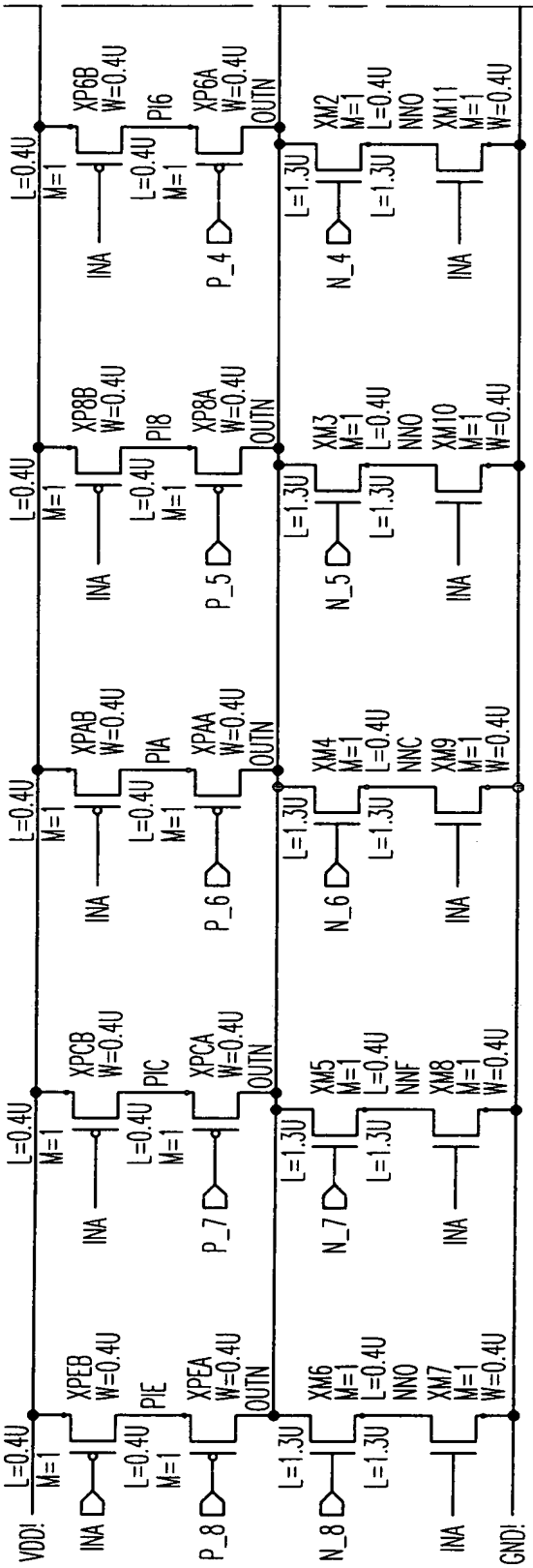

VDD!
GND!
INA
P_8
N_8
P_7
N_7
P_6
N_6
P_5
N_5
P_4
N_4
L=0.4U
M=1
XPEB
W=0.4U
PIE
XPEA
OUTN
XPCB
PIC
XPCA
XPAB
PIA
XPAA
XP8B
PI8
XP8A
XP6B
PI6
XP6A
L=1.3U
XM6
XM7
XM5
XM8
XM4
XM9
XM3
XM10
XM2
XM11
NNO
NNF
NNC

Fig.7-1

300

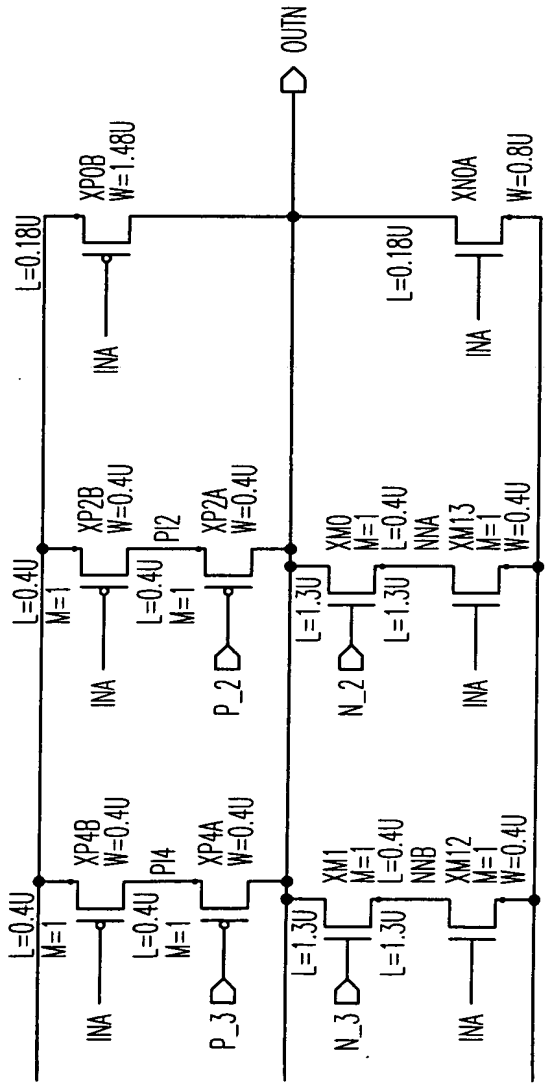

OUTN
XP0B
W=1.48U
L=0.18U
INA
XN0A
W=0.8U
L=0.18U
INA
XP2B
W=0.4U
PI2
XP2A
W=0.4U
L=0.4U
M=1
L=0.4U
M=1
INA
P_2
XM0
M=1
L=0.4U
NNA
XM13
M=1
W=0.4U
L=1.3U
L=1.3U
N_2
INA
XP4B
W=0.4U
PI4
XP4A
W=0.4U
XM1
M=1
L=0.4U
NNB
XM12
M=1
W=0.4U
L=0.4U
M=1
L=0.4U
M=1
INA
P_3
L=1.3U
L=1.3U
N_3
INA

Fig.7-2

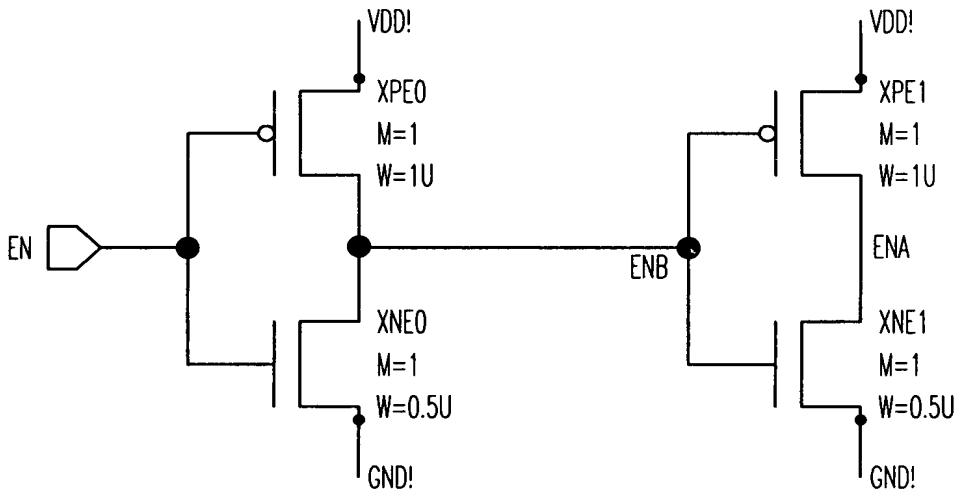

VDD!
XPE0
M=1
W=1U
EN
XNE0
M=1
W=0.5U
GND!
ENB
VDD!
XPE1
M=1
W=1U
ENA
XNE1
M=1
W=0.5U
GND!

Fig.8

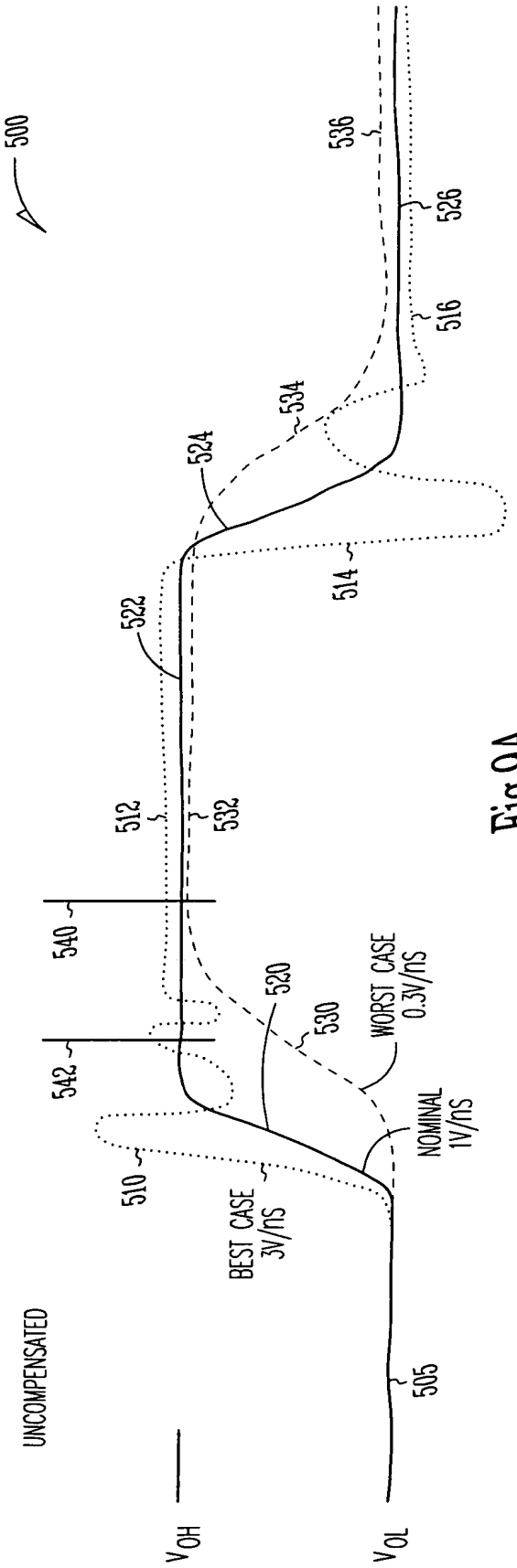

500
536
526
516
534
524
514
522
512
532
540
542
520
530
WORST CASE
0.3V/nS
NOMINAL
1V/nS
510
BEST CASE
3V/nS
505
UNCOMPENSATED
$V_{OH}$
$V_{OL}$

Fig.9A

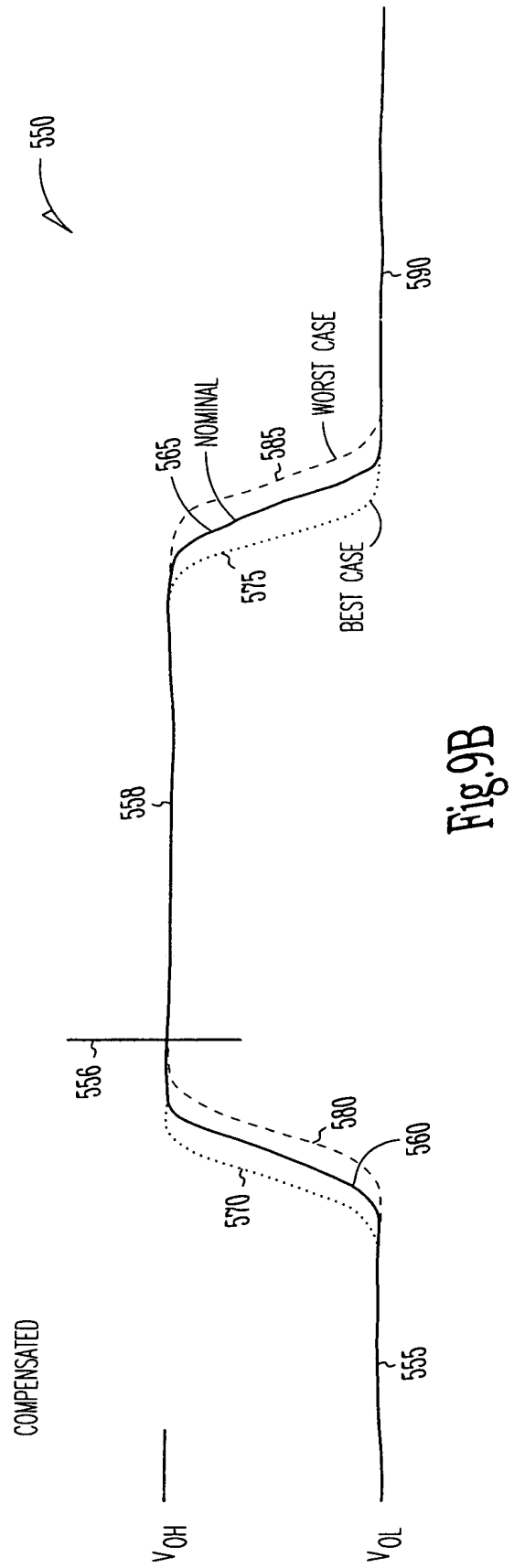

550
590
565
NOMINAL
585
WORST CASE
575
BEST CASE
558
556
580
560
570
555
COMPENSATED
$V_{OH}$
$V_{OL}$

Fig.9B

DESCRIPTION:

NON-INVERTING BI-DIRECTIONAL DRIVER/RECEIVER THAT INTERFACES 1.8V INTERNAL FUNCTIONS WITH 1.1V ENHANCED GTL+ OFF-CHIP BI-DIRECTIONAL DATA BUS. THE DRIVER OPERATES WITH A 1.8V SUPPLY. THE DRIVER HAS OFF-CHIP TERMINATION OF 45 OHM TO 1.1V ($V_{TT}$) AT EACH END OF THE BUS (DOUBLE TERMINATION). THE RECEIVER HAS EXTERNAL REFERENCE Vref ($V_{TT}$*2/3).

| | |
|---|---|
| A0 | DRIVER DATA0 INPUT |
| A1 | DRIVER DATA1 INPUT |
| AN0 | DRIVER DATA0 INPUT |
| AN1 | DRIVER DATA1 INPUT |
| SA | DRIVER DATA SELECT INPUT |
| DI | DRIVER INHIBIT INPUT (DI IN) |
| TS | IN-PHASE DRIVER THREE-STATE CONTROL |
| TSN | OUT-PHASE DRIVER THREE-STATE CONTROL |
| PVTP[8:0] | PMOS EDGE RATE CONTROL BUS INPUT |
| PVTN[8:0] | NMOS IMPEDANCE CONTROL BUS INPUT |
| RE | REFERENCE ENABLE |
| RI | RECEIVER INHIBIT INPUT (RI IN) |
| VREF | (Vtt*2/3) INPUT SIGNAL |
| PAD | IN-PHASE DRIVER OUTPUT/RECEIVER INPUT |
| PADN | OUT-PHASE DRIVER OUTPUT/RECEIVER INPUT |
| ZDI | DRIVER INHIBIT OUTPUT (DI OUT) |
| ZRI | RECEIVER INHIBIT OUTPUT (RI OUT) |
| Z | IN-PHASE RECEIVER OUTPUT |
| ZN | OUT-PHASE RECEIVER OUTPUT |
| ZA | DATA0 TEST OUTPUT (A0 OR A1 OUT) |
| ZAN | DATAN0 TEST OUTPUT (AN0 OR AN1 OUT) |
| ZBSR | PAD TEST OUTPUT (PAD OUT) |
| ZNBSR | PADN TEST OUTPUT (PADN OUT) |
| LT | LEAKAGE TEST INPUT |

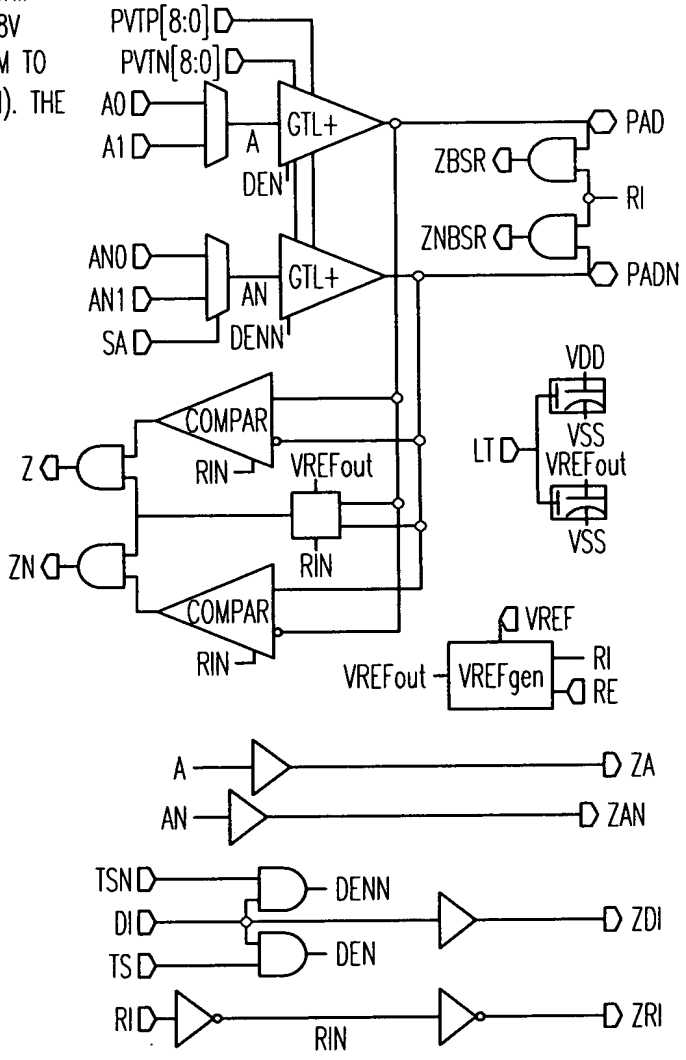



Fig.10

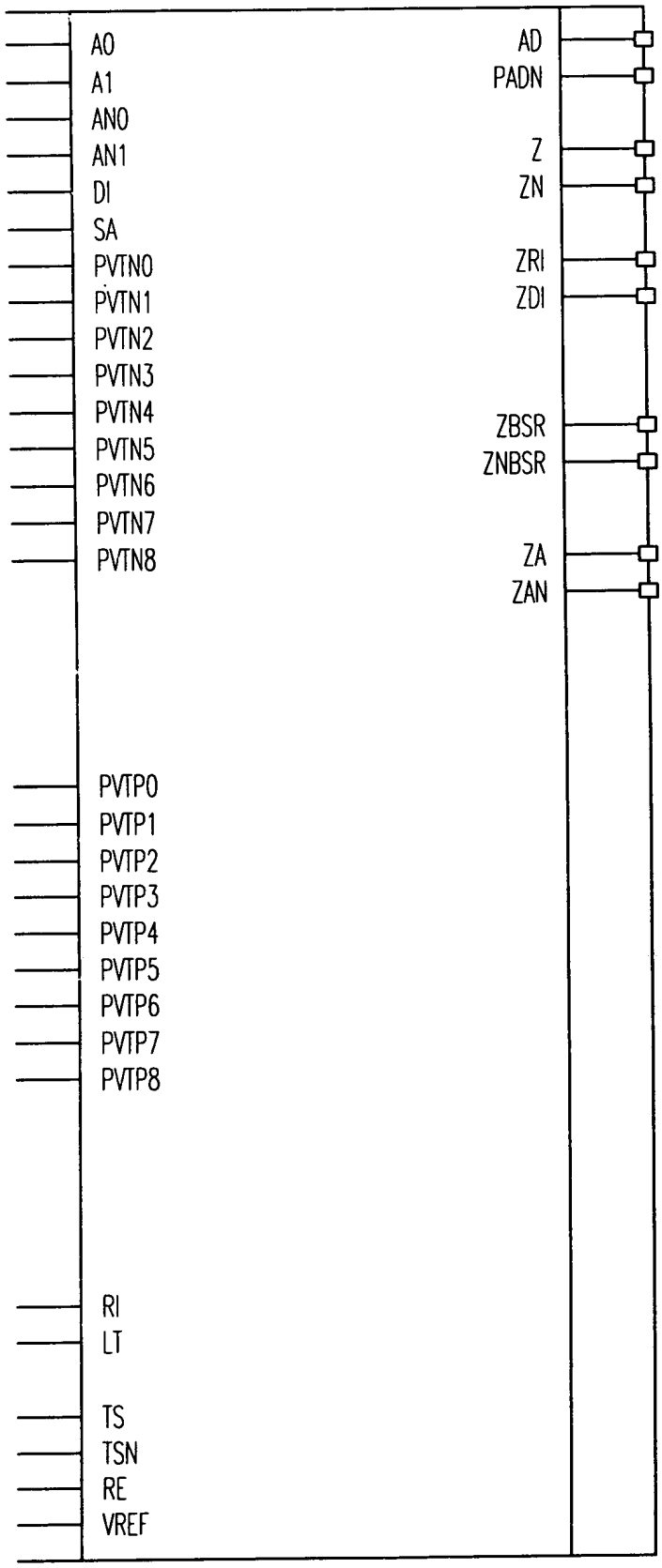

A0
A1
AN0
AN1
DI
SA
PVTN0
PVTN1
PVTN2
PVTN3
PVTN4
PVTN5
PVTN6
PVTN7
PVTN8
PVTP0
PVTP1
PVTP2
PVTP3
PVTP4
PVTP5
PVTP6
PVTP7
PVTP8
RI
LT
TS
TSN
RE
VREF
AD
PADN
Z
ZN
ZRI
ZDI
ZBSR
ZNBSR
ZA
ZAN

Fig.11

DRIVER TRUTH TABLE

| INPUTS | | | | | | | OUTPUS | |
|---|---|---|---|---|---|---|---|---|
| A0 | A1 | SA | TS | DI | PVTP | PVTN | PAD | COMMENTS |
| – | – | – | 0 | – | – | – | HI-Z[1] | HIGH IMPEDANCE MODE |
| – | – | – | – | 0 | – | – | HI-Z[1] | HIGH IMPEDANCE MODE |
| – | – | – | – | – | 0[2] | 0[2] | HI-Z[1] | PVT TEST MODE |
| 0 | – | 0 | – | – | – | 0[2] | HI-Z[1] | PVT TEST MODE |
| 1 | – | 0 | – | – | 0[2] | – | HI-Z[1] | PVT TEST MODE |
| 0 | – | 0 | 1 | 1 | – | >0 | 0[3] | PVT TEST MODE[3] |
| 1 | – | 0 | 1 | 1 | >0 | – | 1[3] | PVT TEST MODE[3] |
| 0 | – | 0 | 1 | 1 | >0 | >0 | 0[3] | FUNCTIONAL, A0 DATA MODE |
| 0 | – | 0 | 1 | 1 | 1 | 1 | 0[3] | FUNCTIONAL, 10 OHMS @ BC |
| 0 | – | 0 | 1 | 1 | 4 | 4 | 0[3] | FUNCTIONAL, 10 OHMS @ NOM |
| 0 | – | 0 | 1 | 1 | 8 | 8 | 0[3] | FUNCTIONAL, 10 OHMS @ WC |
| 1 | – | 0 | 1 | 1 | >0 | >0 | 1[3] | FUNCTIONAL, A0 DATA MODE |
| – | – | 1 | 1 | 1 | >0 | >0 | A1 | FUNCTIONAL, A1 DATA MODE |

1. PAD IS AT "$V_{TT}$" WHEN CONNECTED TO OFF-CHIP TERMINATOR.
2. WHEN PVT=0 ALL PVT BITS GO TO $V_{SS}$ AND ARE OFF.
3. PAD LOGICAL "1"=Vtt=1.1V, LOGICAL "0"=0.4V OR LESS.

NOTES: A. Vdd=1.8(+/-0.1)V, Vtt=1.1(+/-0.02)V

B. DURING MODULE EXTERNAL I/O TEST AND SYSTEM MODE, DRIVER OUTPUT PULLUP IS MADE BY THE EXTERNAL 22.5 OHM RESISTOR TO Vtt.

C. NDR WILL BE BASED ON DRIVER TERMINATED OFF-CHIP.

D. A0, A1, AN0, AND AN1 ARE INDEPENDENT FROM EACH OTHER.

E. ENTRIES IN COLUMNS PVTP, PVTN REPRESENT NUMBER OF LINES HELD AT LOGIC "1" STATE. FOR TESTING, THE IMPEDANCE CONTROLLER FORCES PVTP AND PVTN TO 4 (i.e. PVTP[8:0]=PVTN[8:0]=[000011110]) FOR ALL SUPPLY VOLTAGE LEVELS.

Fig.12

DRIVER TRUTH TABLE

| INPUTS | | | | | | | OUTPUS | |
|---|---|---|---|---|---|---|---|---|
| AN0 | AN1 | SA | TSN | DI | PVTP | PVTN | PADN | COMMENTS |
| – | – | – | 0 | – | – | – | HI-Z[1] | HIGH IMPEDANCE MODE |
| – | – | – | – | 0 | – | – | HI-Z[1] | HIGH IMPEDANCE MODE |
| – | – | – | – | – | 0[2] | 0[2] | HI-Z[1] | PVT TEST MODE |
| 0 | – | 0 | – | – | – | 0[2] | HI-Z[1] | PVT TEST MODE |
| 1 | – | 0 | – | – | 0[2] | – | HI-Z[1] | PVT TEST MODE |
| 0 | – | 0 | 1 | 1 | – | >0 | 0[3] | PVT TEST MODE[3] |
| 1 | – | 0 | 1 | 1 | >0 | – | 1[3] | PVT TEST MODE[3] |
| 0 | – | 0 | 1 | 1 | >0 | >0 | 0[3] | FUNCTIONAL, A0 DATA MODE |
| 0 | – | 0 | 1 | 1 | 1 | 1 | 0[3] | FUNCTIONAL, 10 OHMS @ BC |
| 0 | – | 0 | 1 | 1 | 4 | 4 | 0[3] | FUNCTIONAL, 10 OHMS @ NOM |
| 0 | – | 0 | 1 | 1 | 8 | 8 | 0[3] | FUNCTIONAL, 10 OHMS @ WC |
| 1 | – | 0 | 1 | 1 | >0 | >0 | 1[3] | FUNCTIONAL, A0 DATA MODE |
| – | – | 1 | 1 | 1 | >0 | >0 | A1 | FUNCTIONAL, A1 DATA MODE |

1. PAD IS AT "$V_{TT}$" WHEN CONNECTED TO OFF-CHIP TERMINATOR.
2. WHEN PVT=0 ALL PVT BITS GO TO $V_{SS}$ AND ARE OFF.
3. PAD LOGICAL "1"=Vtt=1.1V, LOGICAL "0"=0.4V OR LESS.

NOTES: A. Vdd=1.8(+/-0.1)V, Vtt=1.1(+/-0.02)V

B. DURING MODULE EXTERNAL I/O TEST AND SYSTEM MODE, DRIVER OUTPUT PULLUP IS MADE BY THE EXTERNAL 22.5 OHM RESISTOR TO Vtt.

C. NDR WILL BE BASED ON DRIVER TERMINATED OFF-CHIP.

D. A0, A1, AN0, AND AN1 ARE INDEPENDENT FROM EACH OTHER.

E. ENTRIES IN COLUMNS PVTP, PVTN REPRESENT NUMBER OF LINES HELD AT LOGIC "1" STATE. FOR TESTING, THE IMPEDANCE CONTROLLER FORCES PVTP AND PVTN TO 4 (i.e. PVTP[8:0]=PVTN[8:0]=[000011110]) FOR ALL SUPPLY VOLTAGE LEVELS.

Fig.13

RIVER PROPAGATION DELAYS (NO LOAD ON OUTPUTS)

| PATH (INPUT TO OUTPUT) | PERFORMANCE LEVEL | PARAMETER | DELAY (ns)=INTERCEOT+SLOPE ($D_{std}$)[1] | | |
|---|---|---|---|---|---|
| | | | $V_{dd}$=1.7[2]V<br>$V_{tt}$ =1.08V<br>$T_j$=100°C<br>PROCESS=SLOW | $V_{dd}$=1.8V<br>$V_{tt}$ =1.1[3]V<br>$T_j$=60°C<br>PROCESS=NOM. | $V_{dd}$=1.9[2]V<br>$V_{tt}$ =1.12V<br>$T_j$=25°C<br>PROCESS=FAST |
| A0-PAD | A | $t_{PLH}$ | 1.2ns | 1.0ns | 0.8ns |
| | | $t_{PHL}$ | 1.2ns | 1.0ns | 0.8ns |
| AN0-PADN | A | $t_{PLH}$ | 1.2ns | 1.0ns | 0.8ns |
| | | $t_{PHL}$ | 1.2ns | 1.0ns | 0.8ns |

1. $D_{std}$ IS THE NUMBER OF STANDARD LOADS.
2. VOLTAGE AT THE PACKAGE PIN.
3. DESIGN IS OPTIMIZED FOR Vtt=1.1V, CAN BE USED FOR Vtt=1.0V TO 1.2V.

Fig.14

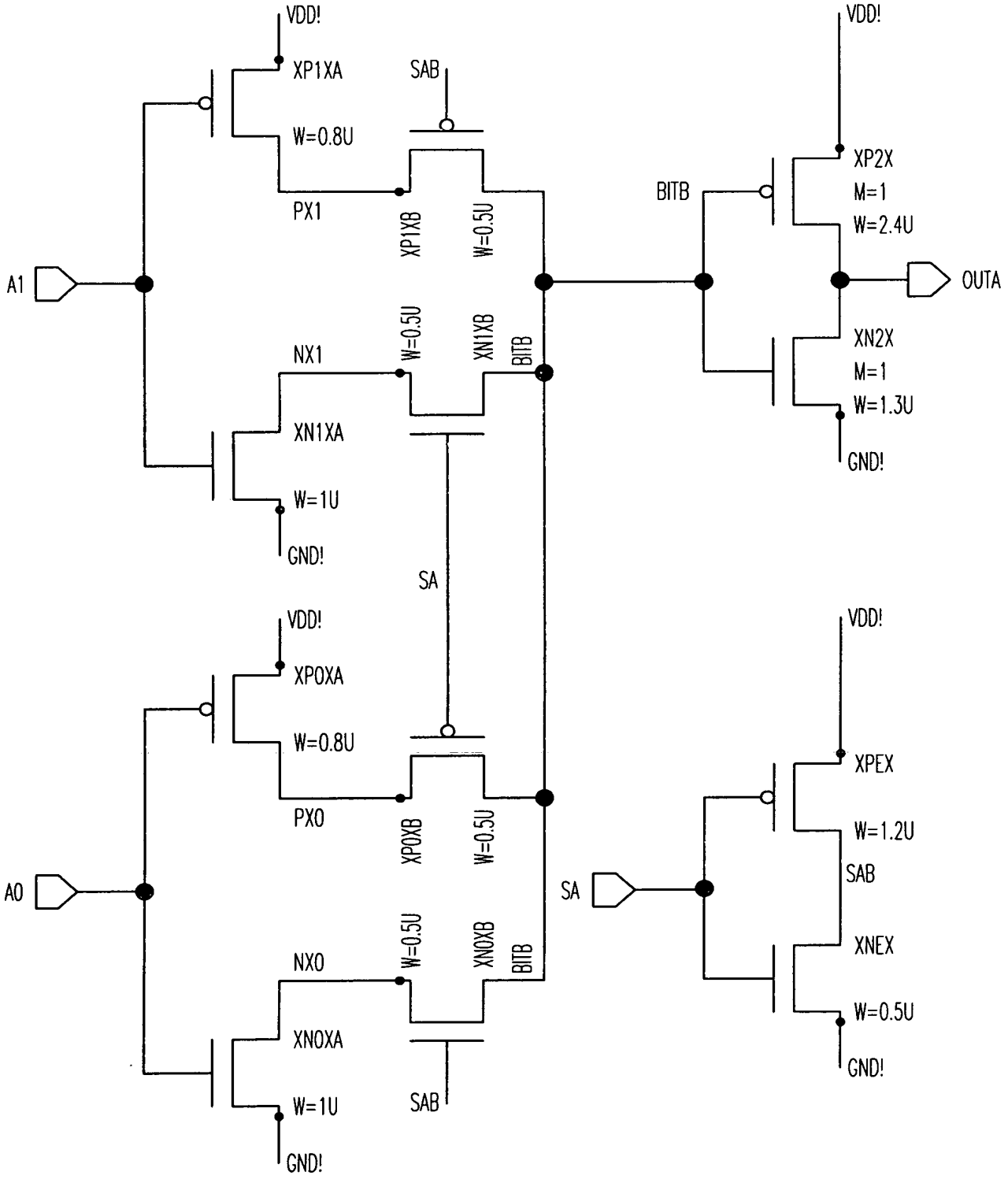

VDD!
XP1XA
SAB
W=0.8U
PX1
XP1XB
W=0.5U
A1
W=0.5U
XN1XB
BITB
NX1
XN1XA
W=1U
GND!
SA
VDD!
XP0XA
W=0.8U
PX0
XP0XB
W=0.5U
A0
W=0.5U
XN0XB
BITB
NX0
XN0XA
W=1U
SAB
GND!
VDD!
XP2X
M=1
W=2.4U
BITB
OUTA
XN2X
M=1
W=1.3U
GND!
VDD!
XPEX
W=1.2U
SAB
SA
XNEX
W=0.5U
GND!

Fig.15